

Communication Solutions



Edition 2006-07-28

Published by Infineon Technologies AG 81726 München, Germany © Infineon Technologies AG 2006. All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.



CONFID	NCA-IP2 Infineon Single Chip Solution for IP Phone CONFIDENTIAL Revision History: 2006-07-28, Revision 1.1 Previous Version:		
Previou			
Page	Subjects (major changes since last revision)		

Trademarks

ABM®, ACE®, AOP®, Arcofi®, ASM®, ASP®, BlueMoon®, BlueNIX®, C166®, DuSLIC®, ELIC®, Epic®, FALC®, GEMINAX®, Idec®, INCA®, IOM®, Ipat®-2, IPVD®, Isac®, Itac®, IWE®, IWORX®, M-GOLD®, MUSAC®, MuSLIC®, OCTALFALC®, OCTAT®, POTSWIRE®, QUADFALC®, QUAT®, SCOUT®, SCT®, SEROCCO®, S-GOLD®, SICAT®, SICOFI®, SIDEC®, SIEGET®, SLICOFI®, SMARTI®, SOCRATES®, VDSLite®, VINETIC®, 10BaseS® are registered trademarks of Infineon Technologies AG.

ConverGate[™], DIGITAPE[™], DUALFALC[™], EasyPort[™], S-GOLDIte[™], S-GOLD2[™], S-GOLD3[™], VINAX[™], WildPass[™], 10BaseV[™], 10BaseV[™] are trademarks of Infineon Technologies AG.

Microsoft[®] and Visio[®] are registered trademarks of Microsoft Corporation. Linux[®] is a registered trademark of Linus Torvalds. FrameMaker[®] is a registered trademark of Adobe Systems Incorporated. APOXI[®] is a registered trademark of Comneon GmbH & Co. OHG. PrimeCell[®], RealView[®], ARM[®] are registered trademarks of ARM Limited. OakDSPCore[®], TeakLite[®] DSP Core, OCEM[®] are registered trademarks of ParthusCeva Inc.

IndoorGPS™, GL-20000™, GL-LN-22™ are trademarks of Global Locate. ARM926EJ-S™, ADS™, Multi-ICE™ are trademarks of ARM Limited.



Table of Contents

Table of Contents

	Table of Contents	4
	List of Figures	5
	List of Tables	6
1 1.1	Introduction	
2 2.1 2.2 2.2.1 2.2.2 2.2.3 2.2.4	Implementation Boot Core BootROM Modules Bootstrap CMD SPI ASC NAND	8 10 10 11
3 3.1	Image Generation	13
3.1.1 3.1.1.1 3.1.1.2	Valid Tokens	13
3.1.1.3 3.1.2	TAG_START	13 14
3.1.2.1 3.1.2.2 3.1.3	FLAG_SDBG	14





CONFIDENTIAL List of Figures

List of Figures

Figure 1	BootROM Exceptions
Figure 2	MPS Memory BootROM Content
Figure 3	Bootstrap CMD Structure
Figure 4	NAND Kernel Boot





List of Tables

List of Tables

Table 1	CPU0 Boot Sources	į
Table 2	CPU1 Boot Sources	
Table 3	MPS Memory BootROM Content	



Introduction

1 Introduction

1.1 Bootable Interfaces

Table 1 describes the interfaces the internal boot ROM code can boot from. In direct boot mode both CPUs access the external FLASH connected to the EBU. The external startup code needs to take care of all startup related issues (exception handling, CPU dispatching). This boot mode is intended as fallback or for special applications. All other boot modes will be supported by the internal boot ROM code. In this mode all exceptions will cause both CPUs to jump to the exception handler located in the ROM by default.

Table 1 CPU0 Boot Sources

CFG(2:0)	Primary	Secondary	Remark
000	EBU		
001	BootROM	ASC0	Serial X-Modem bootstrap
010	BootROM	SPI0 (gen.)	SPI bootstrap, EEPROM command set
011	BootROM	SPI0 (ATMEL)	SPI bootrstrap, ATMEL command set
100	BootROM	EBU NAND (small)	528byte (small page) NAND
101	BootROM	EBU NAND (large)	2112byte (large page) NAND
110	BootROM	reserved	Reserved
111	BootROM	reserved	Reserved
011 100 101 110	BootROM BootROM BootROM BootROM	SPI0 (ATMEL) EBU NAND (small) EBU NAND (large) reserved	SPI bootrstrap, ATMEL commar 528byte (small page) NAND 2112byte (large page) NAND Reserved

Table 2 CPU1 Boot Sources

CFG(2:0)	Primary	Secondary	Remark
000	EBU		
001111	BootROM	SDRAM	Boot vector location read from VRAM

When CFG2:0 equals 000, both CPUs directly boot from external FLASH memory. Since the boot process is handled by the external code completely, this case is not described within this document. Nevertheless CPU0 may change the CFG settings by software, therefore changing CPU1 boot mode. For all cases where CFG2:0 is not equal to 000, both CPUs will fetch instructions from the boot ROM after reset and for certain exceptions.

2 Implementation

2.1 Boot Core

The boot core is written in assembler and takes care of

- MIPS24KEc initialization
- Cache initialization
- CPU exception handling
- CPU dispatch
- · Low-level boot error signalling

All of the BootROM code is executed on exception level, so it is up to the subsequent boot code to take care for entering normal operation. The CPU enters the state "HALT" in case of any unhandled exception, which actually means updating the "BOOT_STATUS" field in the status register (described later on) and entering an infinite loop. In case of an EJTAG exception the CPU executes a DERET in addition to allow usage of the debugger.

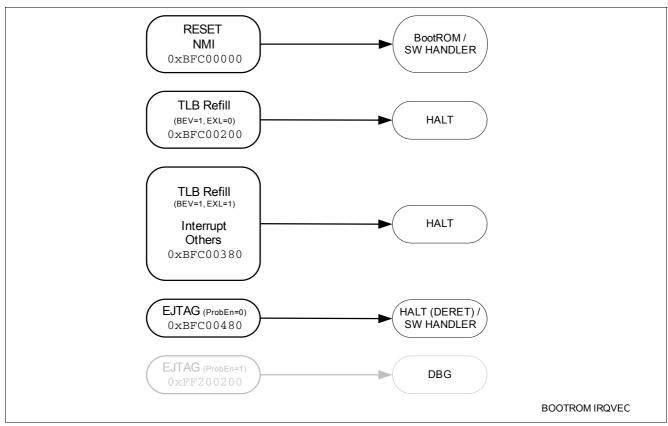


Figure 1 BootROM Exceptions

All information needed by the BootROM is stored in the upmost section of the internal Multi Processor System (MPS) memory. The defined fields and their function are listed in the subsequent table.

Table 3 MPS Memory BootROM Content

Register	Description
BOOT_RVEC	Start address to jump to after reset. Will be filled by BootROM for CPU0 and has to be filled by CPU0 for CPU1.
BOOT_NVEC	Start address to jump to after NMI.



Table 3 MPS Memory BootROM Content (cont'd)

Register	Description
BOOT_EVEC	Start address to jump to after EJTAG exception.
CP0_CAUSE	MIPS CPU register, will be dumped on HALT condition.
CP0_EEPC	MIPS CPU register, will be dumped on HALT condition.
CP0_EPC	MIPS CPU register, will be dumped on HALT condition.
BOOT_SIZE	Only valid for CPU1 - contains the size of the FW code for memory mapping and optional
	decryption. Has to be filled by CPU0 for CPU1.
BOOT_RCU_SR	Only valid for CPU0 - contains the value for register RCU_SR on boot of CPU0.
BOOT_CONFIG	Configuration word latched in during boot (content of RST_SR >> 1), or boot configuration
	tag like read from boot media as soon as first tag is processed.
BOOT_STATUS	BootROM status and error information; should contain latest operation or error code.

The register set is duplicated for both CPUs, resulting in the layout shown in Figure 2.

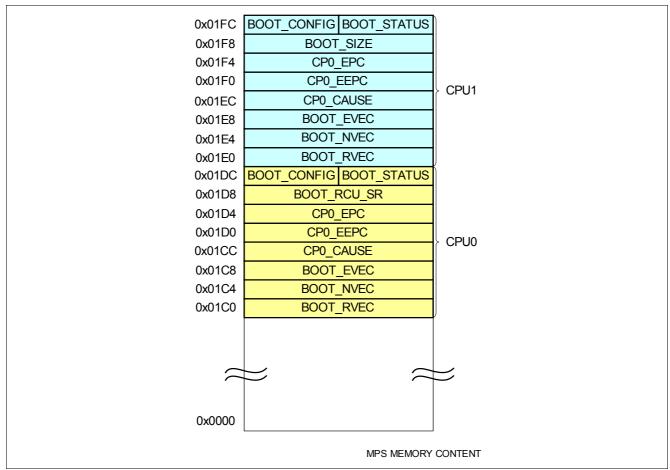


Figure 2 MPS Memory BootROM Content

2.2 BootROM Modules

2.2.1 Bootstrap CMD

Due to the implementation of INCA-IP2 the external boot medium needs to contain information about SDR/DDR SDRAM memory setup before first memory access. Therefore the boot loader expects a special command structure as depicted in following figure. The data format is common for all bootstrap capable interfaces, so that the same binary image can be used independent from the boot source.

The command module accepts three types of commands:

- · Register configuration (REGCFG)
- · Code download (DWNLD to external memory)
- · Start code execution (START)

All commands share a 32-bit tag and the 32-bit length field, containing the number of bytes in the data field. The tag consists of two 16 bit words that add up to 0xFFFF for easy validity checking. The content of the data section is defined by the respective command and described later on.

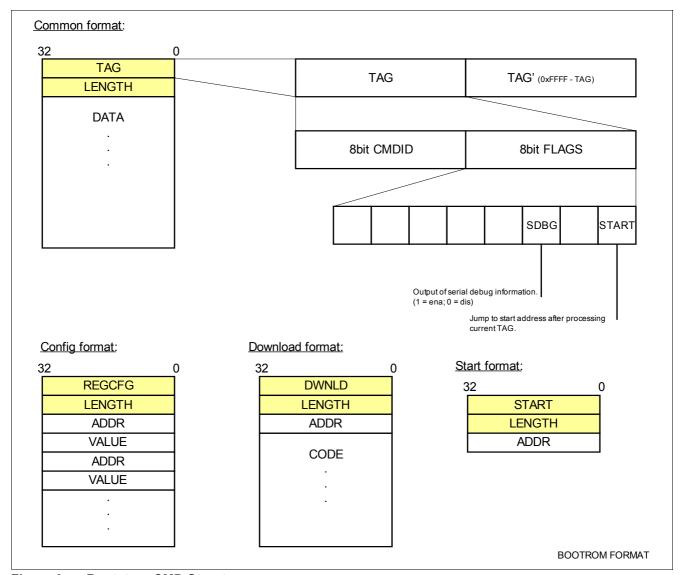


Figure 3 Bootstrap CMD Structure



CONFIDENTIAL Implementation

Register Configuration (REGCFG, CMDID=0x22)

The "REGCFG" command is supplied in order to do SDRAM controller configuration and any other register settings that might be necessary on boot (e.g. workaround). It consists of 32 bit pairs containing register address ("ADDR") and value to write ("VALUE"), which will be parsed sequentially until the number of 32 bit words (stored in "LENGTH") is reached. There is no address verification or value checking implemented.

SDRAM Download (DWNLD, CMDID=0x55)

The download command copies the amount of data specified by field "LENGTH" to the address "ADDR", reading back certain memory locations in order to detect memory failures. The bootloader assumes that the SDRAM has been set up before this command is executed (e.g. using "REGCFG" command).

Code Execution (START, CMDID=0x77)

After successful configuration of the memory interface and downloading the code, the START command will cause the CPU to jump to the specified address.

2.2.2 SPI

The SPI module allows boot strap of devices conforming to SPI mode 0. The default speed of the interface will be limited to 1 MHz to allow booting from all types of devices. To speed up the actual download the maximum supported interface speed can be provided using a small application executed in MPS memory. The separate boot mode for ATMEL devices supports a different commandset (read command 0x8E), while the generic mode will use the wide spread command set where read is represented by "0x03". To achieve compatibility with most devices concerning address length, the loader will probe the number of expected address bytes. This is done by counting the address byte(s) 0x00 following a read command as long as no data is received. Therefore the first byte in serial FLASH memory needs to be different from 0xFF.

2.2.3 ASC

The ASC boot strap uses the X-Modem protocol to download the commands on the serial interface. The default settings of the ASC are 115200 baud, no parity, 1 stop bit. The module either supports standard X-Modem (128 byte frames, simple checksum) or X-Modem 1k (1024 byte frames, CRC16) for higher throughput. Since X-Modem allows up to 1 minute delay after transmitting the first frame, the memory setup commands (REGCFG or IDWNLD) need to fit into the first 128 or 1024 byte depending on used X-Modem speed. This assures that the following transmission succeeds, since X-Modem has no defined flow control.

2.2.4 NAND

The NAND FLASH module allows booting from a standard NAND memory with "guaranteed correct" block 0. The BootROM includes neither ECC checking/correction nor bad block handling algorithms. Therefore the executed software needs to fit into this boot sector (16k for small, 64k for large page NAND) and a two level loader approach needs to be used. The NAND FLASH boot process for a Linux kernel is depicted in the following illustration.

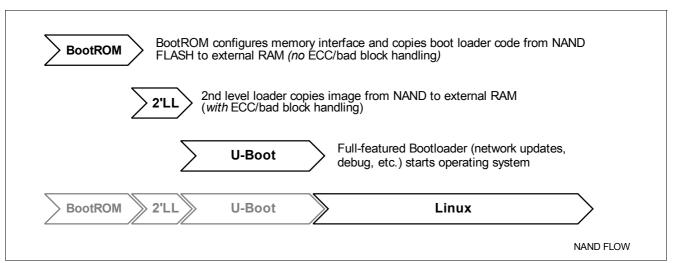


Figure 4 NAND Kernel Boot

Image Generation

3 Image Generation

CPU0 expects to receive the images on the boot strap interfaces compliant to the message format described in the previous chapters. Infineon provides an image generator for converting standard binaries into the format used by the INCA-IP2 BootROM.

3.1 mkbootimg.incaip2

The mkbootimg tool is provided with the INCA-IP2 BSP and can be run on any Linux machine. It has to be called like

```
# mkbootimg.incaip2 <outfile> < <configfile>
```

whereas <outfile> is the name of the image to generate and <configfile> is image description. Please note that the memory controller initialization must be done before issuing any download command and that the register configuration needs to fit into the first block of the used boot interface.

3.1.1 Valid Tokens

The image description language consists of a combination of the following tokens. The tokens may contain single-line comments enclosed with /**/.

3.1.1.1 TAG_REGCFG

The token TAG_REGCFG allows setting one or more internal register(s) specified by <address> to <value>. There is no address validation done in the BootROM.

3.1.1.2 **TAG_DWNLD**

The token TAG_DWNLD allows to download the binary image specified by <filename> (needs to be in quotes, e.g. "image.bin") to the address specified by <address>. The BootROM will halt in case the given address can not be written since the memory controller configuration is invalid. Please make sure that the executable image has been compiled for execution in memory at the same location.

3.1.1.3 TAG_START

The token TAG_START allows to start the binary image at location <address> - the BootROM will perform a direct jump. The BootROM does not check the specified location for valid code.



CONFIDENTIAL Image Generation

3.1.2 Valid Flags

Each of the tokens described above may contain one ore more of the following flags.

3.1.2.1 FLAG_SDBG

The token FLAG_SDBG allows to enable several debug prints on interface ASC0. This option must not be used for X-Modem bootstrap, since the prints will disturb the serial protocol.

3.1.2.2 FLAG_START

The token FLAG_START allows to start the binary <filename> at location <address> after download. The BootROM will be continued after the called routine issues a return instruction.

3.1.3 Configuration example

The following configuration file example will generate an image that

- · configures the memory controller for SDRAM access
- downloads the U-Boot to SDRAM memory
- starts the U-Boot

```
/* Example image file for INCA-IP2 image generator */
/* Don't use multi-line comments...
TAG_REGCFG()
{
   0xBF800060 0x00000006 /* MC_CON
                                         * /
   0xBF800200 0x00000802 /* MC_IOGP
                                         * /
   0xBF800230 0x00000002 /* MC_CFGDW
                                         * /
   0xBF800220 0x00000020 /* MC_MRSCODE */
   0xBF800240 0x000014C9 /* MC_CFGPB0
                                         * /
   0xBF800280 0x00036325 /* MC_LATENCY
   0xBF800290 0x00000C30 /* MC_TREFRESH */
   0xBF8002A0 0x00000000 /* MC_SELFRFSH */
   0xBF800210 0x00000001 /* MC_CTRLENA */
};
TAG_DWNLD()
{
   0x80f00000 "u-boot.bin" /* Download u-boot image */
};
TAG_START()
{
   0x80f00000 /* Start u-boot image */
```



Image Generation

};

The content of the generated image might be (commands marked blue):

```
        0000000:
        2200ddff
        00000048
        bf800060
        00000006

        0000020:
        bf800200
        00000802
        bf800230
        00000002

        0000040:
        bf800220
        00000020
        bf800240
        000014c9

        0000060:
        bf800280
        00036325
        bf800290
        00000023

        0000100:
        bf8002a0
        00000000
        bf800210
        00000001

        0000120:
        5500aaff
        000265f8
        80f00000
        ff000010

        0000140:
        00000000
        fd000010
        00000000
        73010010

        0000200:
        00000000
        75010010
        00000000
        6f010010

        0000220:
        00000000
        6d010010
        00000000
        6b010010

        ...
        0463060:
        e033f280
        0034f280
        3035f280
        10000000

        0463100:
        01000000
        cc01f180
        3435f280
        00000000
```

www.infineon.com Published by Infineon Technologies AG